ISSN: 2093-5374 / E-ISSN: 2093-5382

Hybrid Real-Time Frame and Bit Synchronization for Mixed Signal Data Acquisition System

S. Vinayaka Babu[1*], and Dr.S. Safinaz[2]

[1*]Research Scholar, Department of Electronics and Communication Engineering, Presidency University, Bangalore, India. vinayaka.20223ece0009@presidencyuniversity.in, https://orcid.org/0009-0001-8272-0401

[2]Associate Professor, Department of Electronics and Communication Engineering, Presidency University, Bangalore, India. safinazs@presidencyuniversity.in, https://orcid.org/0000-0003-4245-9664

Received: August 09, 2025; Revised: September 25, 2025; Accepted: October 31, 2025; Published: December 15, 2025

Abstract

This paper presents the design and successful implementation of a hybrid real-time telemetry receiver system based on BPSK demodulation, bit synchronization, and frame synchronization implemented on a Field-Programmable Gate Array (FPGA). The general aim is to eliminate the constraints of traditional analog implementations complexity, size, and tunability by leveraging the FPGA's parallel processing and hardware optimization capabilities. The system introduces novelty by jointly digitalizing various essential elements: a Costas loop with a Digital Controlled Oscillator (DCO) for robust carrier recovery, a timing recovery circuit with the Early-Late Gate algorithm to synchronize bits, and a frame synchronizer with cross-correlation. Moreover, we use 32-bit validation with the Fletcher checksum algorithm to ensure high data integrity and identify transmission errors or corruption. The system can have a flexible range of bit rates from 1 kbps to 64 kbps, with a carrier frequency of 1 MHz and a message signal frequency of 512 kHz. The results indicate that the complete telemetry receiver with a BPSK demodulator has been fully implemented on the Xilinx Virtex UltraScale+. This digital design produces size complexity reduction and better tunability than an analog design. The suggested solution offers real-time performance and superior flexibility in timing for synchronizing and checking data integrity, significantly improving the overall reliability of data receipt and processing in telemetry applications.

Keywords: BPSK, Costas Loop, Bit Synchronization, Frame Synchronization, FPGA, Ethernet, Digital Signal Processing.

1 Introduction

Telemetry has been developed to address the need to relay information over distances where it is not possible to monitor the source of the signal. The essence is that it focuses on the proper transmission of information between remote or distant places, facilitating communication and information transfer.

As shown in Figures 1 and 2, a telemetry system can be broadly divided into two primary functional subsystems. A source portion with transducers, a source-signal processing section with multiplexing and conditioning signal, and a transmitting section make up the transmitting subsystem. The receiving

Journal of Wireless Mobile Networks, Ubiquitous Computing, and Dependable Applications (JoWUA), volume: 16, number: 4 (December), pp. 115-135. DOI: *10.58346/JOWUA.2025.I4.007*

*Corresponding author: Department of Electronics and Communication Engineering, Presidency University, Bangalore, India.

system comprises several components, including receiving antennas, preamplifiers, receivers, magnetic recorders, demodulators, data or bit synchronizers, data processors, and displays (Kommangunta et al., 2022; Zhang et al., 2013). It should be noted that all these elements are required to guarantee the data quality captured at the receiving subsystem.

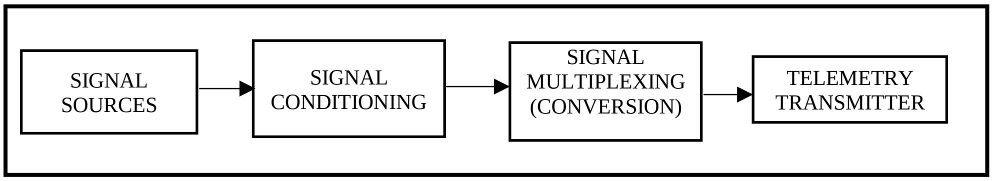

Figure 1: Telemetry transmitting system

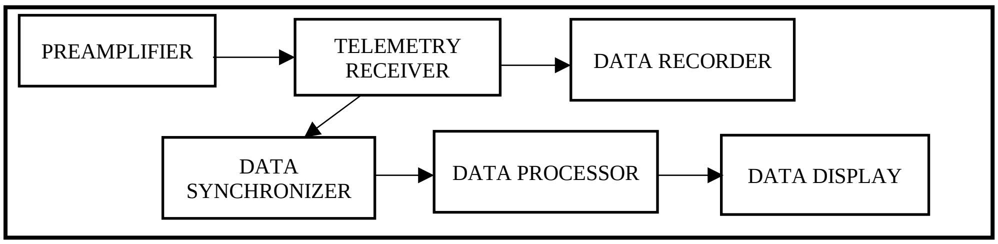

Figure 2: Telemetry receiving system

Pulse code modulation (PCM) is commonly used in contemporary spacecraft to transmit binary data between mission control and the spacecraft. Binary data is expressed by phase modulation of an RF carrier using PCM/PM, or by modulating the phase of a subcarrier with a pulse or a 90-degree phase shift. The subcarrier is subsequently modulated further by phase modulation onto the carrier signal, thus facilitating efficient transmission through the space link. The application of PCM enables accurate, secure data transmission in spacecraft communications.

The telecommunications industry has experienced tremendous growth in installations due to the greater flexibility of digital communication systems compared to analog systems (Asha et al., 2024; Awad et al., 2021). Due to its benefits, including reduced hardware design complexity, higher bandwidth efficiency, and enhanced signal-to-noise ratio, Phase Shift-Keying (PSK) has gained widespread popularity as a digital transmission method. PSK encodes the carrier wave to convey data, and Binary Phase Shift Keying (BPSK) is a popular one-dimensional modulation method in which the carrier phase is shifted by 180° for each data symbol. (Bondariev et al., 2020; Al-Makhles et al., 2013).

Accurate carrier frequency and phase information becomes essential at the receiver's end for coherent synchronous demodulation (Rezvani et al., 2025; Flammini & Ferrari, 2010). The modulated BPSK signal does not have a distinct spectral line at the carrier frequency, yet displays a dense spectral distribution around it (Kumar et al., 2022). To retrieve phase and frequency information from the received signal and ultimately produce a sinusoidal reference signal, carrier recovery circuits are essential (Scofield et al., 2019; Braojos et al., 2016). The circuits in question are classified as closed-loop systems.

This study employs the most recent design methodologies to implement a Costas loop, a closed-loop carrier recovery circuit (Dubey & Thakur, 2024; Batista et al., 2002). The Costas loop, invented by John Costas, is a variation of the Phase Locked Loop (PLL) used to lock onto and demodulate signals whose carrier has been suppressed, such as those used in some types of AM radio. It works by using two PLLs that operate 90 degrees out of phase with each other (Desai & Joshi, 2023; Sousa et al., 2006).

The conventional analog signal method suffers from imbalances between the quadrature-phase and in-phase components and faces implementation challenges. Digital Costas loops offer a solution by directly transforming analog components into discrete time. The use of the Costas loop in a Field-programmable gate array (FPGA) offers benefits in terms of complexity, size, and tunability (Yang & Fathy, 2009; Li et al., 2022).

We apply a Costas loop with direct synthesis and make use of the CORDIC algorithm. The CORDIC algorithm is commonly used when multipliers are constrained and must be implemented using simple operations such as addition and subtraction. However, since modern FPGAs have a built-in multiplier, the CORDIC algorithm can be generalized to cases where computational power is higher; we choose to include it in our design of a direct digital synthesizer or digital-controlled oscillator (DCO) (Sondej & Bednarczyk, 2024; Shah et al., 2019).

In this implementation, we compute loop parameters using formulas, which can lead to a gap between theory and practice. Therefore, there was no possibility of comparing theoretical and practical simulations. And the whole system is implemented on a single FPGA, with the phase detectors using a digital multiplier and the digital low-pass filters implemented using the least-squares method. The system's main oscillator uses Direct Digital Synthesis (DDS), and the required control is provided by a digitally controlled oscillator (DCO). Furthermore, cosine filtering is applied with a user-defined roll-off factor (Shrivastav & Malakar, 2024).

The results of the cosine filtering operation are then sent through an Automatic Gain Controller (AGC) to obtain quantized outputs. For bit synchronization, a timing recovery algorithm with two samples per bit is employed. This algorithm accurately synchronizes the receiver's sampling clock with the transmitted bit stream based on two samples per bit interval.

For error-decoding algorithms that might identify errors within the received data stream, Reed-Solomon (RS) codes are applied (Chauhan & Bhatia, 2025; Sumithra et al., 2019). Used in conjunction with convolutional codes, these codes provide excellent performance with minimal bandwidth increase, especially at high signal-to-noise ratios. The output stage of the convolution decoder may be set to code the data into NRZ-L format if a telemetry waveform was used on the RF channel.

The bit synchronizer uses an early gate scheme to synchronize with the received data stream (Mei et al., 2022) accurately (Li et al., 2019; Lazarovych et al., 2021). For data integrity verification, a 32-bit verification process compares each bit to a pre-specified reference in a systematic manner. When all 32 bits are the same, the data is accepted. Any variation, however, sends a red flag, which allows appropriate management of such an occurrence.

This technology ensures reliable data transmission through a variety of strategies. It performs bit and frame synchronization to place the received data in the correct location, assembles it according to Ethernet protocols, and conducts a 32-bit validation to verify the data. The effectiveness and dependability of such a system have been established through simulation and empirical testing and can thus be implemented across the broadest range of communication applications (Desai & Iyer, 2024; Abdallah et al., 2011).

2 Background Study

In (Ahmad et al., 2022), Ahmad et al. developed a new non-coherent binary phase-shift keying (BPSK) demodulator, DeepDeMod, based on a deep neural network (DNN). It has been claimed that this innovation enhances demodulation under suboptimal conditions, such as fading channels, additive white Gaussian noise, and hardware imperfections like phase and frequency offsets. Also, the authors address time-varying channel conditions and hardware variations by extending DeepDeMod with transfer learning. With this setup, pilot symbols are transmitted along with the data to tune the DNN and ensure demodulation accuracy. The authors have also applied DeepDeMod to a software-defined radio (SDR) platform and empirically given results. The paper is also relevant to mixed-signal data-acquisition systems, including those that use software-defined radio, as it shows that deep learning can improve demodulation efficiency in harsh conditions. The use of pilot symbols to enable real-time adaptation of the demodulator may be crucial to the design of robust synchronization techniques (Agarwal & Yadhav, 2023).

Blackburn et al., 2023 describe the design and simulation of an activation phase synchronizer for AQFP circuits. AQFP circuits are known as superconducting multi-phase logic circuits activated by a multi-phase activation signal. The phase synchronizer is designed to synchronize input data to a pre-specified phase for the following cycle, which removes clock skew and allows asynchronous designs with unknown data arrival times. The paper proposes a weak constant QFP cell for implementing the phase synchronizer. The cell then filters the input signal to prevent the Synchronizer from amplifying random noise. The authors also provide a simulation of the phase synchronizer circuit, initial fabrication, and test results of the weak cell of constant QFP.

Pan et al., 2021 in studied the problem of high data rate and low bit-error rate (BER) in terms of data telemetry and effective wireless power transfer of small, implantable flexible electronics. These novelists present a telemetry system, which is self-powered and requires only two coils to power it and deliver the information with the assistance of binary phase-shift keying (BPSK) modulation. A phase-locked loop (PLL)-based demodulator can be implemented digitally and is one of the most desirable elements of its implementation. The digital assistance improves the functionality of the PLL and consequently enables the non-traditional data rates that are not restricted by the PLL bandwidth. The system can therefore attain data rates up to 2.26 Mbps and a rate of less than 8.6 x 10 -5 BER simultaneously. The work can also be used by the mixed-signal data acquisition systems as it provides a solution to the concurrent transfer of data and power; therefore, the emphasis is on the simultaneous high data rate and low errors. Of particular interest is the digital-assisted PLL demodulator, which offers a solution to the bandwidth limitation of the traditional PLL-based demodulators, which may pose a problem in the development of fast data acquisition systems.

Chaichomnan & Khumsat, 2023 propose a demodulator with a single-phase phase-locked loop (PLL) for BPSK/QPSK signals. This contribution is interested in the use of a rising-edge RESET/SET flip-flop (RSFF) phase detector. The design is helpful since it possesses a linear characteristic that is advantageous for phase control. The demodulator in the proposal is modular, i.e., it can be extended to higher-order PSK modulation schemes (Arvinth, 2024). The researchers fabricated the BPSK and QPSK demodulators using a 0.18 μm CMOS fabrication process, with the achieved symbol rates being 25 Mbps and 12.5 Msymb/s, respectively, at a carrier frequency of 60 MHz, with power consumption of 0.68 mW and 0.79 mW, respectively. The symbol-error rates at these mentioned data rates were found to be below 7.9 x 10^-10 and 9.8 x 10^-10, respectively. The manuscript also contains a theoretical analysis of the symbol-error rate of the proposed demodulation architecture (Ojha & Arora, 2024; Majid et al., 2024).

Malik et al., 2014 described the design and implementation of a binary phase-shift keying (BPSK) modulator and demodulator in the hardware description language VHDL. The article highlights the trustworthiness, safety, and effectiveness of digital communication over analog communication. The authors used a BPSK modulator and demodulator on a Spartan 3E, FPGA development kit. The study applies to mixed-signal data acquisition systems because it outlines the execution of a BPSK modem, which is a key component of digital communication systems that pass data by modulating the phase of a carrier wave. The BPSK modulation and demodulation are widespread in systems that transmit digital data using a physical channel, and the VHDL implementation offers a hardware view that can be applicable to the design of data acquisition systems.

This paper examines the procedure of adding a BPSK demodulator, or in other words, a bit and frame synchronization procedure, to a telemetry reception system. It successfully shows how a functional system with the use of FPGA technology can be used, which is real-time and adaptive. The above design takes advantage of the parallelism inherent in FPGAs to provide effective and reliable synchronization and checking of the integrity of the data. The benefits of this FPGA method are dimensional, complexity, and configurability compared to the traditional analog design.

3 Proposed Methodology

Figure 3 demonstrates the suggested approach to the telemetry receiver/recording station.

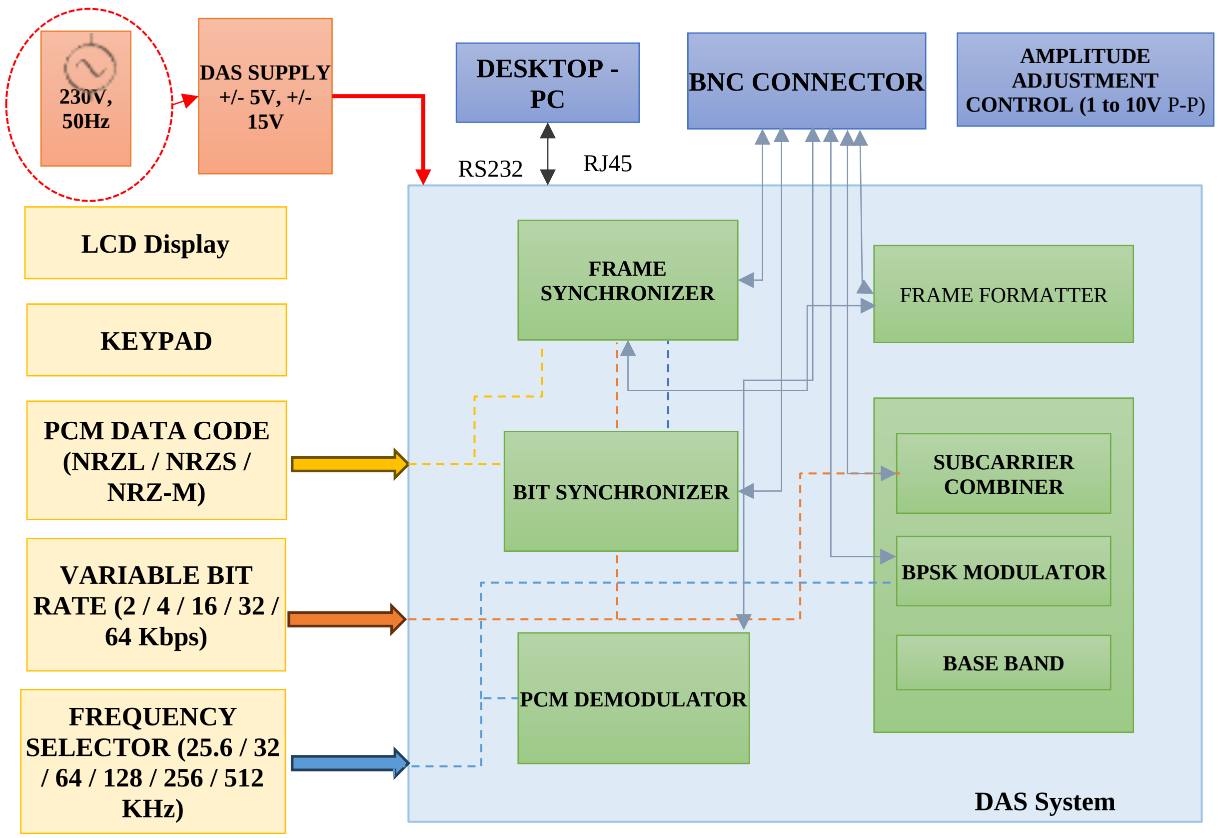

Figure 3: Proposed telemetry receiver /recording station

a. PSK Demodulator

BPSK demodulator at 1 MHz carrier frequency and 512 kHz message signal frequency, on an FPGA (Sourabh et al., 2019) (Figure 4).

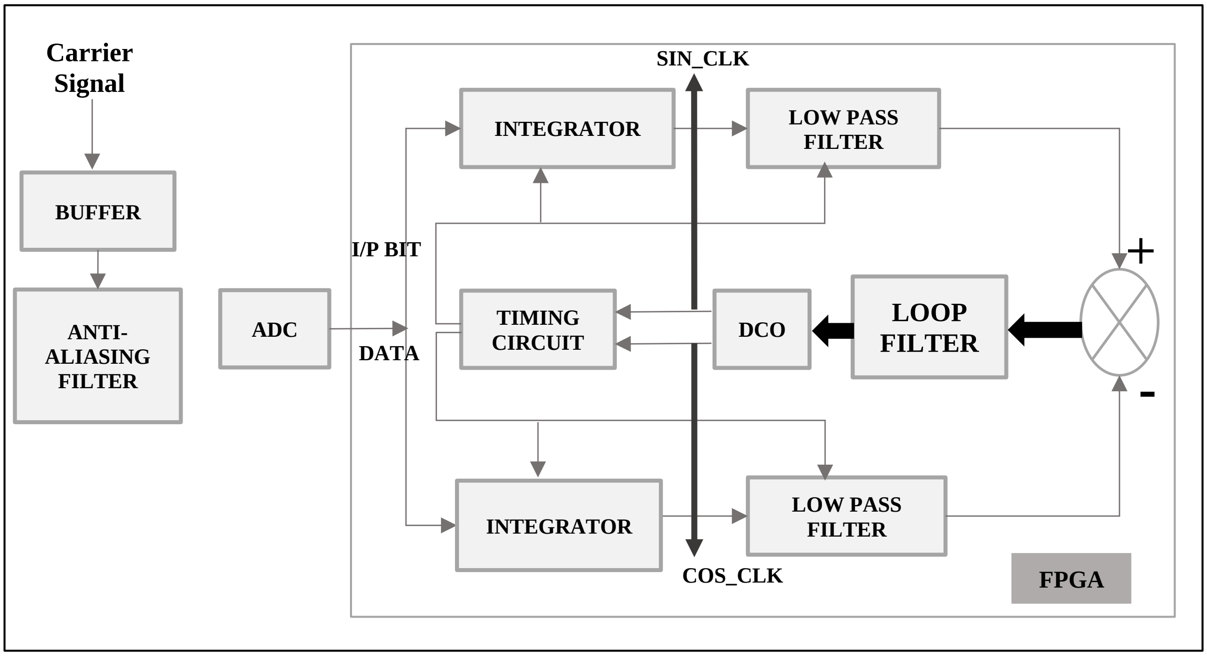

Figure 4: Block diagram of PCM/BPSK demodulator

ADC (Analog to Digital Converter): ADC samples an analog BPSK modulated signal at a given sampling rate and converts it to discrete digital values (Malik et al., 2014). This could be mathematically described using the equation below:

$$\text{digital\_sample} = \text{round}(\text{analog\_sample} * (2^\wedge N\text{-}1)) \qquad (1)$$

Where,

- analog_sample is the analog value sampled.
- N is the number of bits of the ADC resolution,
- and digital_sample is the quantized digital value.

Antialiasing Filter: An antialiasing filter avoids aliasing occurrences while sampling.

Timing Circuit: The Timing circuit extracts the timing information from the received BPSK signal.

The procedures that are involved in the sampling time involve an early-late gate algorithm, in which the maximum likelihood estimation of the most appropriate sampling time is obtained.

Performing the quantization as carried out by the Analog to Digital Converter (ADC) can be explained by equation(1). It does the conversion of the continuous analog signal, analog_sample, into the scale over which the ADC can actually perform owing to its N-bit resolution. The rounding operation is of the utmost importance, and converts the scaled figure 4 to a digital representation, which is discrete and quantized, and which introduces a quantization error that is necessary in the further digital processing.

DCO (Digital-Controlled-Oscillator): This DCO produces a local carrier signal and may have its frequencies changed. The mathematical equation of this can be written as:

$$\text{carrier\_signal}\ (t) = \cos\ (2 * \pi * \text{carrier\_frequency} * t) \qquad (2)$$

Where,

- carrier_signal (t) is the carrier signal generated at time t, and

- carrier_frequency is the signal.

Equation (2) models the ideal local carrier signal generated by the Digital-Controlled Oscillator (DCO) for synchronous demodulation. It represents a pure sinusoid with a frequency adjustable by the DCO control word. In a coherent receiver, the instantaneous phase and frequency of this signal, carrier_frequency, must precisely match the received signal to effectively down-convert the BPSK signal to the baseband.

Loop Filter (carrier recovery): This loop filter is used to filter the error signal of the carrier recovery loop. The equation of the loop filter depends upon the design and can be a combination of proportional, integral, and derivative terms.

Low-Pass Filter (for baseband signal): The low-pass filter is employed to eliminate high-frequency noise from the demodulated baseband signal.

Integrator: The integrator sums up the filtered baseband signal over time. The integrator equation would be:

$$\text{Integral\_value}(t) = \text{integral\_value}(t-1) + \text{filtered\_signal}(t) \quad (3)$$

Where,

- integral_value (t) is the accumulated value at time t,
- filtered_signal (t) is the filtered baseband signal at time t.

Equation (3) represents the digital realization of an accumulator or integrator for the baseband signal. At each time step t, the current sample, filtered_signal(t), is added to the previous accumulated sum, integral_value(t−1). This has the effect of applying matched filtering, which maximizes Signal-to-Noise Ratio (SNR) prior to the decision to make a bit.

The channel signal that enters is demodulated, i.e., it is passed through a low-pass FIR filter. This isolates the continuous signal of amplitude ±1/2 against the demodulated signal and can then select to zero frequency signals (+1/2 or -1/2). One is performed using a comparison block to give one's and zero voltage levels, as well as avoiding the distortion of pulses.

The BPSK demodulator takes a carrier signal of 1 MHz and accepts the digital signal of the modulator as input (Lee et al., 2021). It amplifies the input signal to the carrier signal with a mixer. The demodulator has two major blocks: carrier recovering with the help of the symbol timing recovery and the Costas loop with the help of the algorithm Early Late gate.

A raised cosine filter is used to enhance the quality of the demodulated signal, with a roll-off of 0.24. A mixer, loop filter, and digitally controlled oscillator give carrier signal recovery in a Costas loop. Lastly, automatic gain control (AGC) is used to process the signal to provide a constant level of output that can be easily used in subsequent digital processing (Reddy & Mohan, 2024).

The role of the BPSK demodulator is to demodulate an incoming signal that was BPSK-modulated so as to recover the original data (Ahmad & Agarwal, 2023). To understand what this is done, one has to understand the techniques of BPSK demodulation, like phase ambiguity resolution and the quality of recovered data, which is judged by calculating the rate of bit errors.

Costas-loop: Costas-loop is one of the methods of carrier signal recovery, and it involves the use of a mixer, a low-pass filter (LPF), and a Digital Controlled Oscillator. The recovery of carriers is required because the receiver is usually unaware of what the phase is. The carrier signal can be detected using the mixer output through the use of a Costas loop and DCO. The algebraic steps that simplify the output of the loop's multiplier/phase detector to show the resulting Phase Error Signal (e(t)) is proportional to sin(2△φ), where △φ is the carrier phase error.

The derivation must show the signal output of the phase detector and the algebraic steps that simplify it to the Phase Error Signal ($e_{carrier}$):

$$e_{carrier}(t) \approx k_p \cdot \sin(2\Delta\varphi)$$

Digital Controlled Oscillator (DCO): Coherent receiver design requires carrier recovery due to the uncertainty inherent in the actual carrier phase and frequency of the carrier signal that was transmitted. Voltage-controlled oscillators (VCOs) were employed to adjust the carrier frequency accurately in analog systems based on the outputs from the phase-detection circuits. In digital systems, a digitally controlled oscillator accomplishes this adjustment, thus making it possible to control the carrier phase accurately in Figure 5.

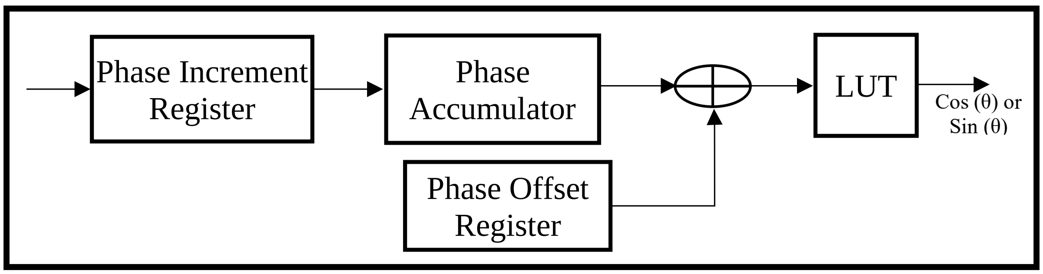

Figure 5: DCO implementation diagram

Phase Increment Register: Every clock cycle adds a value (Δ) to the accumulated phase, which is stored in the phase increment register. The output signal's frequency is determined linearly by the phase increase. Frequency shift keying modulation frequently uses this input. The phase increment is dynamically obtained from an input port, based on the configuration of the digitally controlled oscillator (DCO). The output frequency is consistently a fraction of the system's clock frequency.

Phase Accumulator: The phase accumulator calculates the phase angle value used to access the lookup tables for generating the output sine signal. The phase angle at each cycle is determined by adding the phase increment to the phase angle of the previous cycle. The width of the accumulator for cycle i is determined by the user-defined parameter "Phase resolution". When the phase increment is set to 1, the phase resolution is maximized for a given accumulator width. As the phase increment exceeds 1, the phase resolution decreases.

Phase Shift Keying: The accumulated phase is adjusted by adding a constant phase input before accessing the lookup table. This feature is handy in the implementation phase of the shift keying modulation of the output from the digitally controlled oscillator. The quantizer module scales down the production of the phase accumulator to reduce the size of the lookup table. By utilizing the quantizer, fractional phase increments can be achieved, even when the resolution is limited to integers.. The width of the quantizer determines the depth of the lookup table, and it's typically smaller than the width of the phase accumulator output.

Lookup Table: A key component of the digital-controlled oscillator is a lookup table that stores values of the sine wave for evenly spaced phase angles within the (0, 2π) interval. Depending on the size of the wave parameter, the lookup table can store sine wave samples for the (0, π) interval or the (0, π/2) interval if "half" or "quarter" is selected, respectively. By manipulating the address, the cosine value can be obtained from the same lookup table.

b. Bit Synchronizer

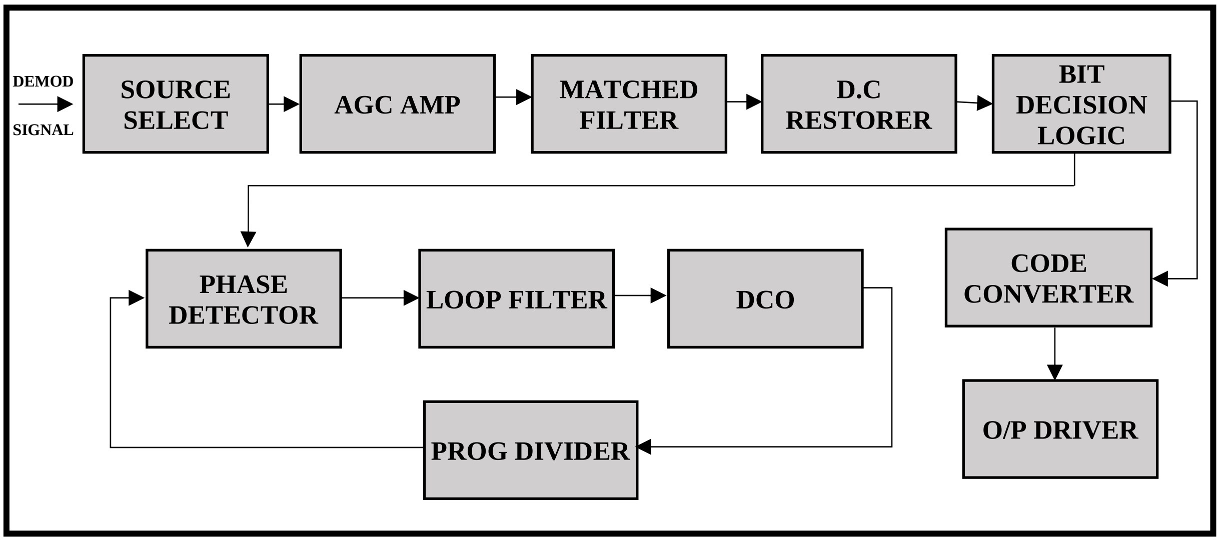

Figure 6: Block diagram of bit synchronizer

Automatic Gain Control (AGC): The AGC serves to adjust the gain or amplification of a signal to maintain it within a desired range. The AGC gain is a control parameter that determines the amplification level applied to the input signal. By multiplying the AGC gain by the input signal, the AGC output is obtained, which represents the adjusted signal with the desired level of amplification as in Figure 6.

$$AGC_{out} = AGC_{gain} * AGC_{in} \quad (4)$$

Where,

- AGC_{in} is the input signal AGC_{gain}
- AGC_{gain} is the gain value determined by the AGC algorithm.

The Automatic Gain Control (AGC) (Equation (4)) is a feature that guarantees that the signal amplitude is kept at a constant and desirably optimal level (AGCout) to be used in digital processing. This is done through dynamically computing and multiplying the input signal (AGCin) and the AGC gain. A constant amplitude is needed to ensure stable operation of follow-on blocks such as the decision logic and the timing error detector, particularly in channels with varying signal strength.

Matched Filter: It is possible to obtain the output of the matched filter by convolution between the input signal and the filter coefficients.

$$\text{Matched Filter}_{out} = \text{Convolution (inpusgnla, FilterCoefficients)} \quad (5)$$

The following operation (5) is the essence of the Matched Filter, and it is significant to the task of maximizing SNR at the sampling time. The convolution is an artificial multiplication of the signal that the transmitter sends with a reversed and shifted copy of the pulse shape (symbolized as FilterCoefficients). The output of this process, Matched Filter out, is the best signal output to be used in the detection of symbols.

DC Restorer: The signal resulting from the subtraction of the average signal of the input signal is called the DC-restored signal:

$$\text{DC\_Restored\_out} = \text{Input Signal - Average (Input Signal)} \quad (6)$$

DC Restorer (Equation (6)). The unwanted DC bias that can be introduced by the channel or receiver front-end to teach and otherwise bias the bit decision threshold is eliminated through the application of equation (6) DC Restorer. The result of subtracting the calculated Average (Input Signal) from the Input Signal itself results in the output, DC restored, centered about zero, so that the next comparator threshold will appropriately indicate the boundary between the 1 and 0 symbols.

Bit Decision Logic: The binary value determined by the height of the input signal relative to a threshold is determined by bit decision logic. It can be represented as:

$$\text{Decision} = 1 \text{ if Input Signal} >= \text{Threshold, else Decision} = 0 \quad (7)$$

The Bit Decision Logic is the simple yet basic equation (7). It is a significant process in which the continuous and filtered input signal is divided into its final binary counterpart. The amplitude of the signal is compared to a signal value against the Threshold (preferably zero in BPSK) so as to determine the recovered data bit (Decision). This is a non-reversible processing stage that converts the soft value into complex binary data to process it further.

Phase Detector: A phase detector is used to measure the difference between the received signal and the local oscillator. And the phase error may be calculated as

$$\text{Phase\_Error}= \text{atan2 (Imaginary)(InputSignal)Real (LocalOscillator) -Real (InputSignal) Imaginary (LocalOscillator), Real (InputSignal) Real (LocalOscillator) + Imaginary (InputSignal) Imaginary (LocalOscillator))} \quad (8)$$

The Phase Error of a complex phase detector has been given by the formula (8), which is frequently determined by multiplying the local oscillator complex input signal by the conjugate of the local oscillator. In order to obtain a consistent phase difference at all four quadrants (with zero negative), the use of the arctan2 function is required. The calculated error is then passed to the loop filter and corrects the phase of DCO.

Loop Filter: The output of the loop filter may be calculated by means of a proportional-integral (PI) controller:

$$\text{LoopFilter\_out} = \text{Kp*Phase\_Error} + \text{Ki Integral (Phase\_Error)} \quad (9)$$

The Proportional-Integral (PI) Loop Filter is a typical model, which is represented as the equation (9), and it attempts to manipulate the Phase Error in order to generate the DCO control word. The proportional term (Kp) needs less time and is immediate in correcting, but the integral term ($Ki \cdot \int$) eliminates steady-state errors, thus correcting proper frequency and phase locking. Kp and Ki are the constants that will be required to determine the bandwidth and the damping factor of a loop.

Programmable Divider: The Output frequency of a programmable divider is calculated using this equation:

$$\text{Divider\_frequency} =(\text{Input\_frequency}) / N \quad (10)$$

Where,

- N is the programmed value for division.

The Programmable Divider equation (10) calculates the output frequency by dividing the high-frequency input frequency (typically the system clock or reference clock) by the programmed integer division factor, N. This circuit is essential in synchronizers for generating the required lower frequency clock signals (e.g., the symbol clock) from a single, high-frequency reference.

Code Converter: The code converter transforms the digital data into an appropriate format for subsequent processing. The algorithm employed in the code conversion ensures that the data is represented in the desired binary format.

The demodulated, received data stream from the receiver undergoes filtering, resulting in a processed signal that is the original data. The serial High-speed data are often transmitted without an accompanying clock signal.

c. Frame Scynchronizer

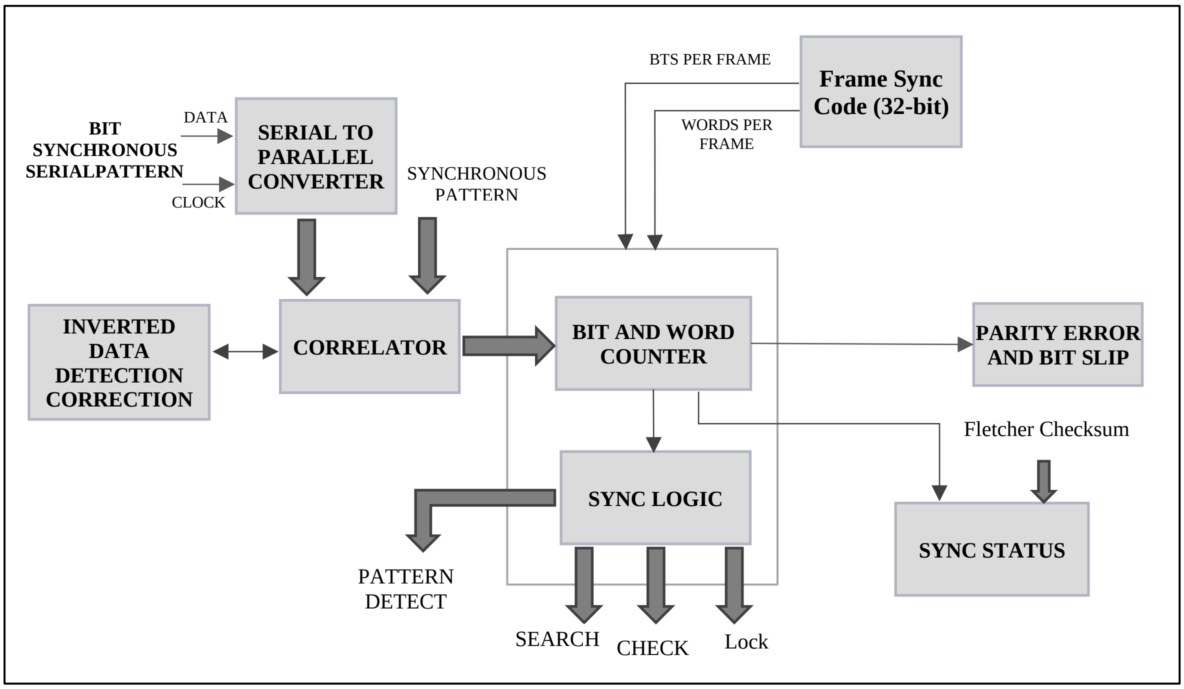

Figure 7: Block diagram of frame synchronizer

To recover the clock signal from a received digital data stream, the system first calculates the difference in phase between the incoming signal and a locally generated clock. This difference is then averaged, and the results are used to adjust the timing of the local clock so that it coincides with the incoming data in Figure 7.

Two primary ways of restoring the timing of symbols are open-loop and closed-loop. In open-loop techniques, the clock signal of the received data is extracted using techniques that emphasize the transitions between symbols. On the contrary, closed-loop approaches constantly compare the local clock with the received information and make adjustments to ensure the two are in tandem.

There are two types of closed-loop synchronizers: in-phase and mid-phase. Both of them have integrators that are used to determine the behavior of the signal in the change of the data. The measurements are then applied to control a digitally controlled oscillator, which is eventually synchronized.

The early-late Synchronizer is comprised of two gated integrators responsible for integrating the signal within specific time intervals. The early gate integrates the signal before the expected data transitions, while the late gate integrates these signals right after the transition. These gate intervals are adjacent to each other and will not overlap. In the absence of timing error, the data transitions precisely align with the boundary between the early and late gates. Here, k represents the counting index within the sequence data pulse.

The derivation must define the Timing Error Detector (TED) output, e_{timing}, and show its relationship to the timing offset (τ):

$$e_{timing} = X_{KE} - X_{KL}$$

And demonstrate how e_{timing} = 0 only when the local timing is perfectly aligned with the incoming bit transitions.

$$\mathrm{X_{KE}} = \frac{1}{T_1}\int_{\tau+(K-(\frac{1}{2}))T}^{\tau+KT} S(t)dt \qquad (11)$$

$$\mathrm{X_{KL}} = \frac{1}{T_1}\int_{\tau+KT}^{\tau+(K-(\frac{1}{2}))T} S(t)dt \qquad (12)$$

The above equations (11) and (12) define the Early (X_{KE}) and Late (X_{KL}) signal samples by integrating the received signal, S(t), over adjacent half-bit intervals (T_1) around the nominal K-th symbol boundary τ+KT. The Early integral accumulates energy just before the transition, while the Late integral accumulates energy just after. The difference between these two values forms the timing error signal used to drive the DCO, ensuring the local clock aligns perfectly with the data transitions.

The integration time constant determines the behavior of integrators. Taking into account resource utilization and simplicity, the early-late closed-loop synchronization method is an optimal choice. Figure 8 illustrates a fundamental block diagram of an early-late synchronization. A time reference point is established via a locally generated square wave clock from the DCO. When the DCO square wave is perfectly synchronized with the demodulation signal, both the early integrator and the late integrator will accumulate an equal amount of energy, resulting in a zero error signal. If the DCO frequency exceeds that of the demodulated signal, the demodulation signal is delayed via Δ, and the DCO frequency is increased while its timing is advanced to align with the incoming signal.

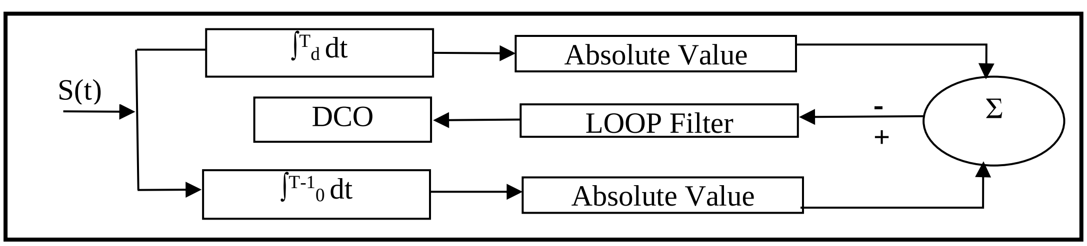

Figure 8: Early-late synchronizer

The Fletcher checksum algorithm, developed by John G. Fletcher at Lawrence Liver Labs in the 1970s, is designed to provide error-detection capabilities similar to a cyclic redundancy check (CRC) but with less computational complexity using summation techniques in Figure 9.

The Fletcher checksum is computed by performing a modular sum of the checksum values for each block of data. The modulus used for the computation is the same throughout. Starting with both sums initialized to zero (and another known value), each block data word is sequentially added to the first sum, and the updated first sum is added to the second sum. Finally, the modulus operation is applied, with two sums combined to result in the Fletcher checksum value.

The order of blocks affects the checksum calculation, with one block added to the first sum; then subsequently added to the second sum along with all the blocks that follow it. If two adjacent blocks are inadvertently swapped, the resulting checksum will be different. Although the final value of the first sum remains unchanged, the second sum reflects a modification, thereby detecting the alteration in the message.

As a result, the Fletcher checksum expands the possible checksum. In this example, where each sum has 255 possibilities, the combined checksum has a total of 65,025 possible values.

Fletcher-32 checksum**:** The Fletcher checksum algorithm operates by dividing the data word into 16-bit blocks, generating two 16-bit sums, and then combining them to create a 32-bit checksum. In the standard Fletcher-32 variation, the second sum is typically multiplied by 216 and added to the simple checksum. This results in sums being combined into a 32-bit word, with the simple checksum positioned at the least significant end. When calculating the Fletcher-32 checksum, the decision to use the modulus, 216 -1 = 65535, is usually explained. The same reason was used to choose the Fletcher-16 checksum.

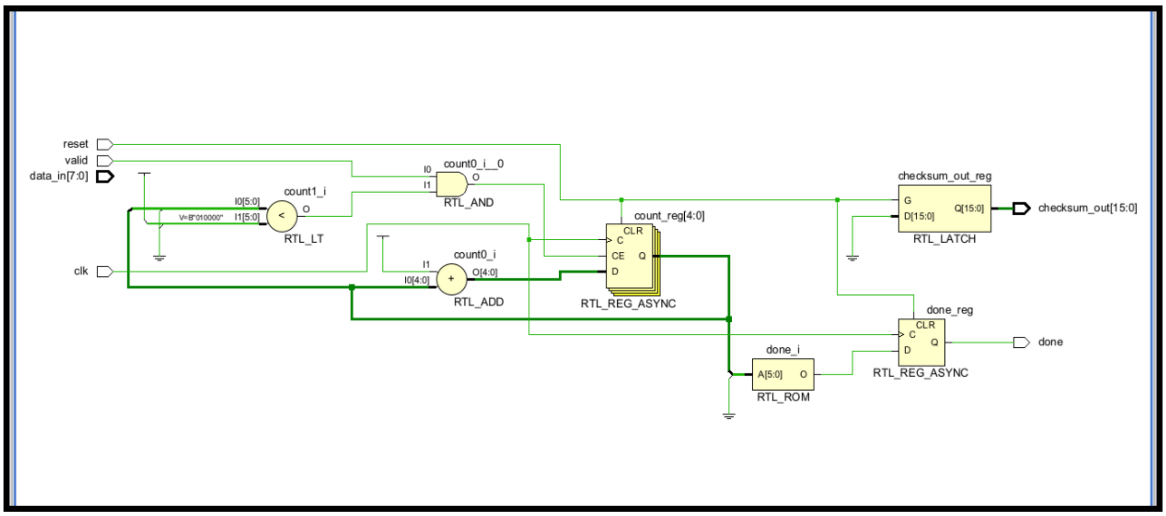

Figure 9: Block diagram of fletcher checksum

d. Data Source – Frame Formatter

Frames of the system, such as the Frame Formatter module, Figure 10 Data Source, are some of the major modules. It can be programmed to communicate with a display and a microcontroller, and is handy for the input of 32-bit data. After the frame synchronization has been achieved, the module passes the PCM telemetry data processor to run Decommunization and generate display parameters.

The frame synchronizer uses a number of modes to synchronize and date the frames appropriately, i.e., SCAN, CHECK, VERIFY (Authenticate), and LOCK. These modes are essential in making sure that there is appropriate synchronization.

The output of the module is sent over the Ethernet, where the communication process is facilitated easily, and the processed telemetry data can be transferred easily.

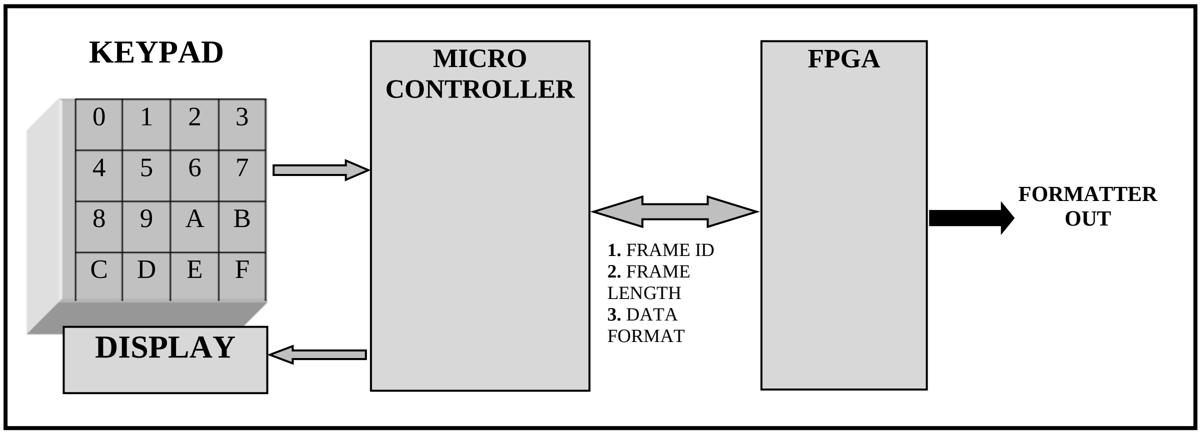

Figure 10 : Block diagram of data source – frame formatter

4 Simulation Results

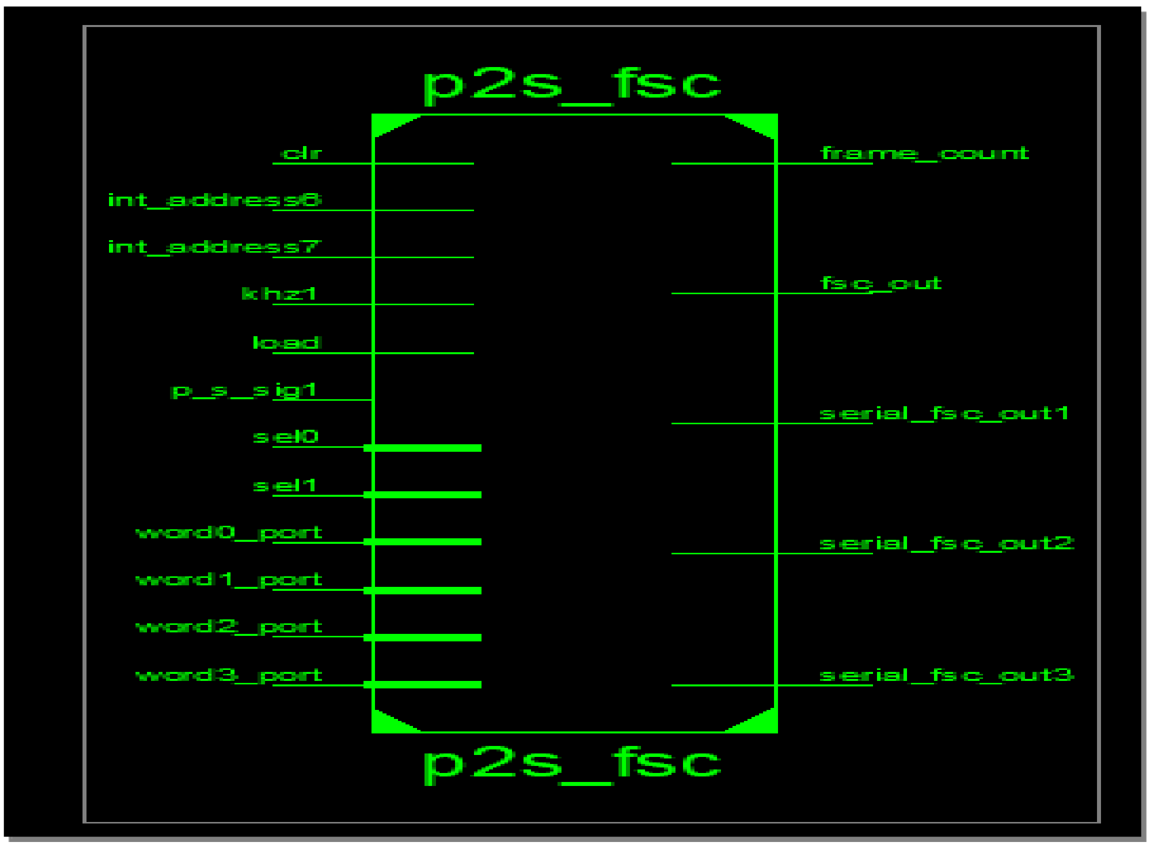

Figure 11: Frame synchronizer

Just as in Figure 11, parallel-to-serial conversion of data frame synchronization is the least around the circuit. Digital communications are systems that need parallel data reassembled and transmitted serially. The frame synchronizer assists the receiver in recognizing a source and a mark of each of the data frames to be viewed in such a way.

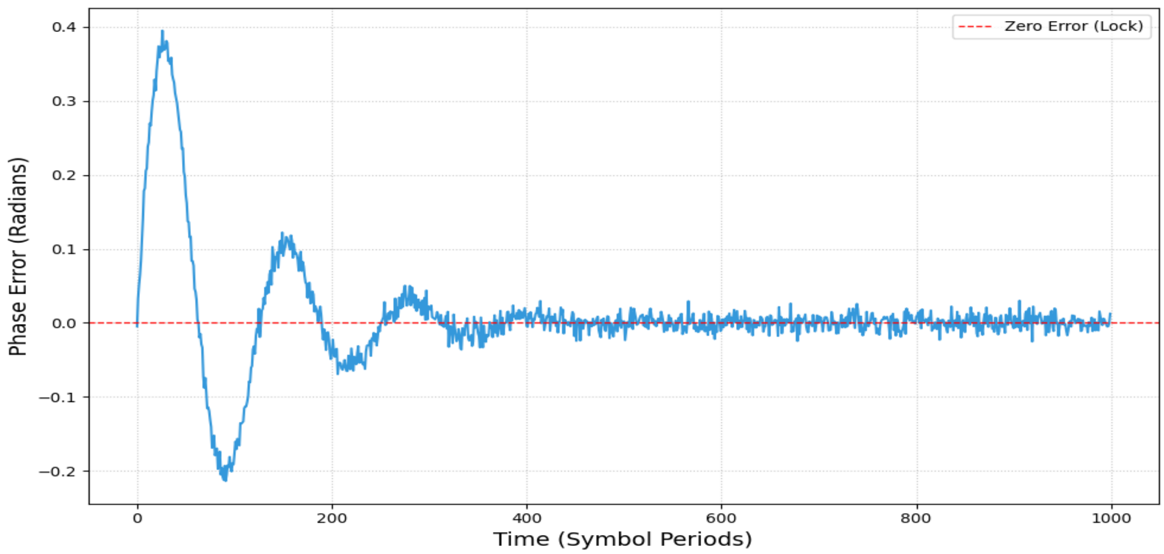

Figure 12: Costas loop phase trajectory and convergence

Figure 12 illustrates the dynamic specifications of the all-digital Costas Loop throughout the procurement of the carrier. The angular distance between the carrier acquired and the local Digital Controlled Oscillator (DCO) is the phase error, implying. It is a massive mistake, and temporary, as it is characteristic of the acquiring period, that are denoted in the loop diagrammed. The proportional-integral (PI) loop filter corrects this error immediately by making the DCO vary in frequency and phase, and the error reforms itself to zero (the red dashed line). The soundness of the PI controller parameter (Kp, Ki) design is determined by the unchangeable convergence of the first periods of the X symbols, the carrier lock obtained is correct, and is required to get the proper demodulation of BPSK.

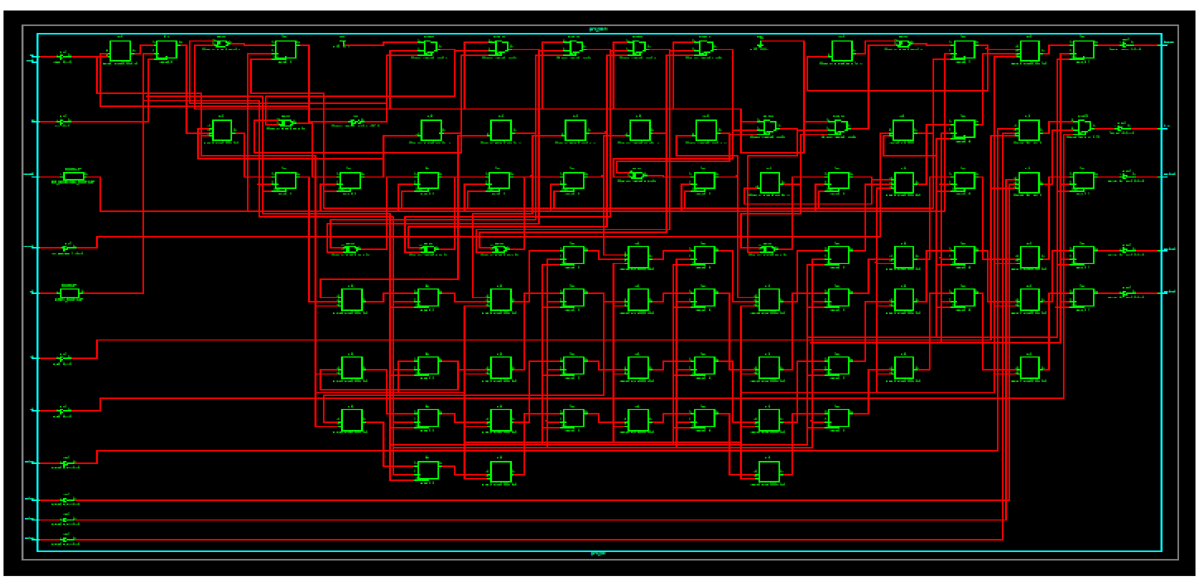

Figure 13: RTL: Schematic diagram for frame synchronizer

Figure 13 RTL schematic: The software architecture of the hardware of the Frame Synchronizer as implemented in the integrated modules of the FPGA. These primitive variables are the shift register, which is the movement of the incoming data, and the cross-correlator block, which makes a comparison of the data with the saved discrete word template. The state machine manages the search (SCAN), detection (CHECK/VERIFY), and lock (LOCK) modes with the help of the correlation peak output to calculate frame alignment.

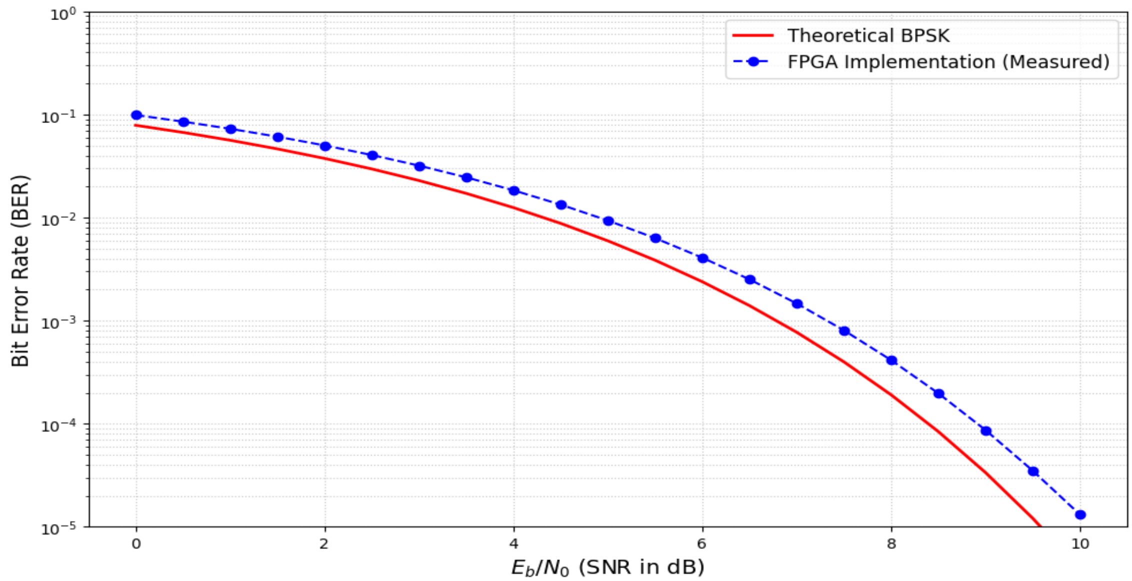

Figure 14: Bit error rate (BER) performance vs. SNR

The performance analysis of the whole receiver chain is a plot of the measured Bit Error Rate versus the other values of Signal-to-Noise Ratio (SNR) as shown in Figure 14. The red solid curve is the theory of ideal performance of BPSK modulation by the Additive White Gaussian Noise (AWGN). The blue dashed line contains the markers of the implementation of the BER in the FPGA. The effectiveness of the digital demodulator, the Costas loop, and the Early-Late Gate synchronizer is confirmed by the fact that measured and theoretical curves are rather coincidental. The low degradation has confirmed that there is no deterioration in material performance on the applied quantization, filtering, and decision processes, and this is what has led to the revelation that the system is very robust and the quality of the operations is also of high quality.

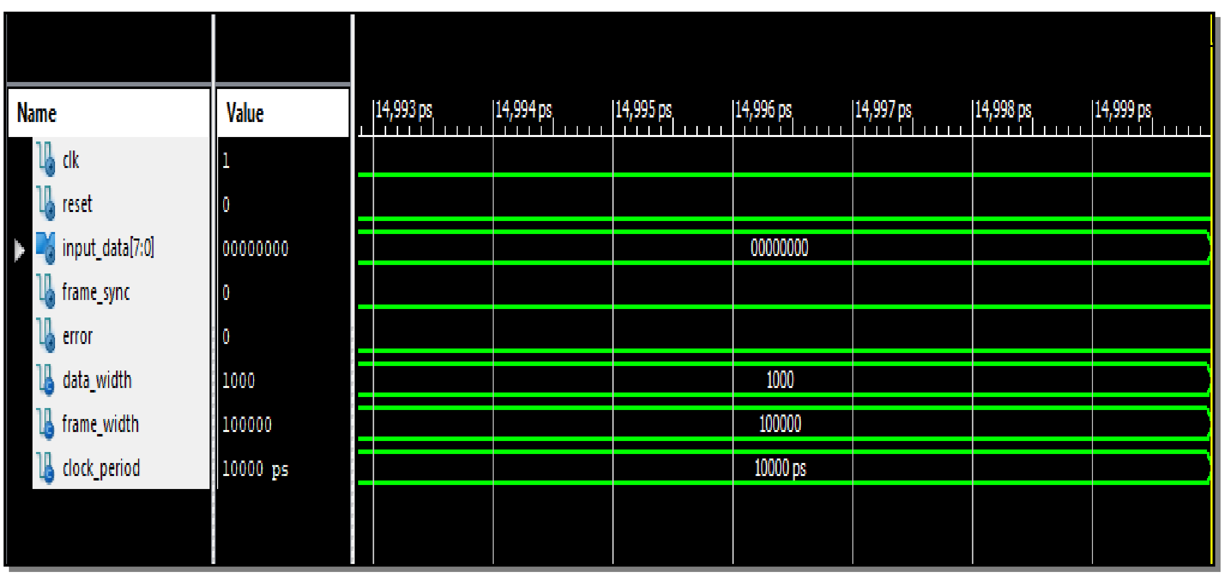

Figure 15: Frame synchronizer waveform

The changes in the critical state that are observed in the Figure 15 waveform indicate that there is sound frame synchronization. It also describes the turning of the system, which is based on the mode of searching Unique Word (SCAN mode), to the mode of Check and Verify in the event of the preliminary match of correspondence. Better still, the waveform is a final attempt to adjust the LOCK mode after the confirmation requirements, which signaled the permanent frame adjustment. The fact that this timing trace shows that the logic of the state machine is correct demonstrates that the system can limit frame boundaries in the right way.

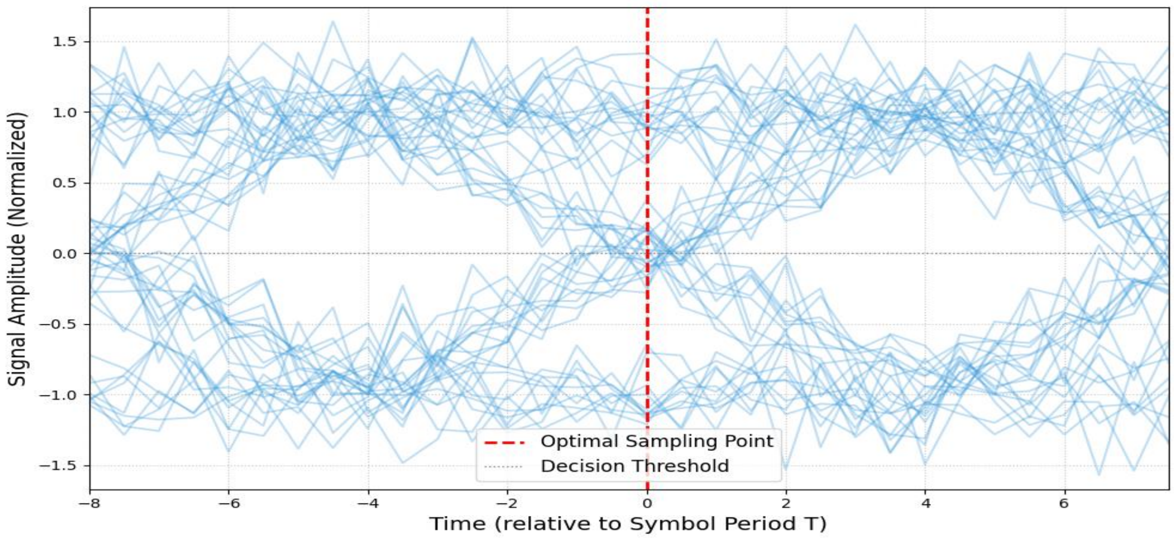

Figure 16: Eye diagram after matched filter (synchronized)

Figure 16 shows the diagram of the eyes, which is an essential qualitative analysis of the success of the bit synchronizer and the channel. It is a pull-out of the signal from the matched filter to a signal being received, and the segments of the signal are superimposed with the symbol clock, which has been selected by the receiver. This huge aperture of the center of the figure suggests that there is not much inter-symbol-interference (ISI), and the received signal is good. T /2 (marked by the red dashed line) is the optimum vertical difference, the optimum point where the decision block should sample the extracted signal that has been extracted successfully and stored within the time frame successfully with the help of the Early-Late Gate algorithm.

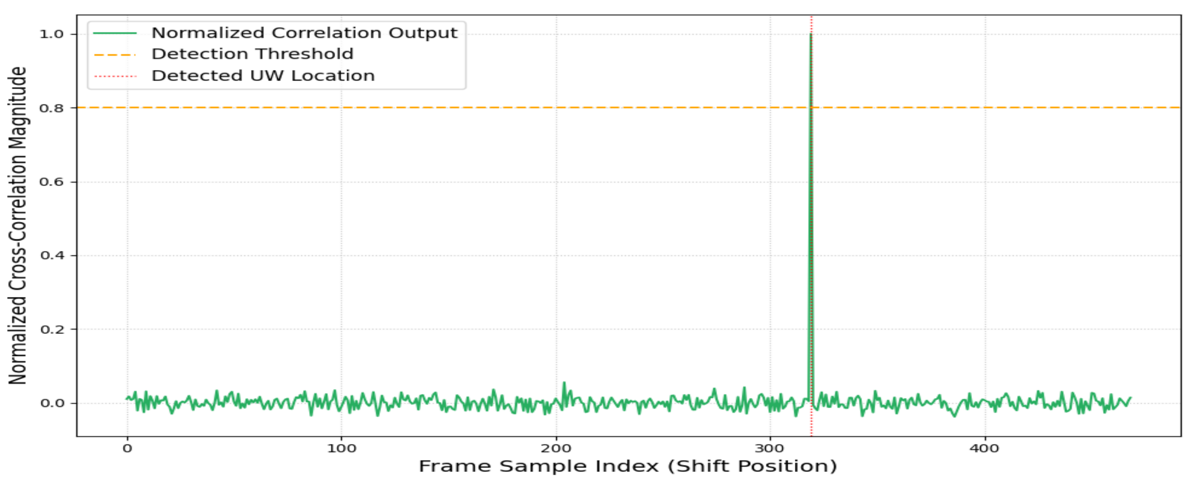

Figure 17: Cross-correlation output for frame synchronization

The main idea of the Frame Synchronizer core functionality is visualized in Figure 17, and the authors rely on the cross-correlation algorithm that is used to identify the known Unique Word (UW) sequence that is embedded in the data stream. The magnitude of the correlation is still low as the receiver moves the UW sequence through the incoming data (indicated by the Sample Index), resulting in the random data matching. There is a single, clear peak at the index of 350 that obviously surpasses the predefined detection threshold (orange dashed line). This maximum value has validated a close correspondence between the local UW and received data, enabling the system to appropriately lock onto the data frame beginning and appropriately execute the next data integrity test (Fletcher Checksum).

Simulation Interpretation

The circuit is shown in the simulation without being reset. The 8-bit input is also noted at 14,996 ps, which shows the processing of data. The frame sync signal is not asserted, indicating that no frame boundary has been passed and no frame sync is beyond this view. No errors are observed. Data parameters that the circuit operates on are determined as constant data width and frame width.

To do this thoroughly, we should monitor the simulation over a longer duration and compare the frame video of these signals: frame_sync, input data, and frame width. Also, we need to possess some knowledge of how the circuit operated, presumably the frame synchronizer, to be able to read the waveforms. Frame_sync should be a pulse at the beginning or the end of the frame, as specified in frame-width.

5 Conclusion

To sum up, this paper has introduced the effective installation of a telemetry receiver system which uses the FPGA technology and specifically the Xilinx Virtex UltraScale+ FPGA. The system has a BPSK demodulator, bit synchronization, and a frame Synchronizer that allows the system to receive and process data reliably. The FPGA-based design has big size, complexity, and tunability advantages over the analog designs.

The Virtex UltraScale+ FPGAs offer high-performance processing units and programmable logic units, as well as vast I/O units required to facilitate the intricate functionality of the telemetry receiver mechanism. This is supported by integrated high-speed transceivers, large on-chip memory, and DSP capabilities that allow maximally effective execution of carrier recovery, timing recovery, and verification of data integrity.

The practical implementation of the whole system on a single FPGA demonstrates the efficiency of the suggested method, which puts the feasibility of using FPGA-based implementations in attaining reliable and accurate data capture and processing in telemetry in the spotlight.

References

[1] Abdallah, M., Elkeelany, O., & Alouani, A. T. (2011). A low-cost stand-alone multichannel data acquisition, monitoring, and archival system with on-chip signal preprocessing. *IEEE transactions on instrumentation and measurement*, *60*(8), 2813-2827. https://doi.org/10.1109/TIM.2009.2036402

[2] Agarwal, A., & Yadhav, S. (2023). Structure and Functional Guild Composition of Fish Assemblages in the Matla Estuary, Indian Sundarbans. *Aquatic Ecosystems and Environmental Frontiers*, *1*(1), 16-20.

[3] Ahmad, A., & Agarwal, S. (2023, January). Demonstrating deep learning driven bpsk demodulation using software-defined radios. In *2023 15th International Conference on COMmunication Systems & NETworkS (COMSNETS)* (pp. 180-182). IEEE. https://doi.org/10.1109/COMSNETS56262.2023.10041280

[4] Ahmad, A., Agarwal, S., Darshi, S., & Chakravarty, S. (2022). DeepDeMod: BPSK demodulation using deep learning over software-defined radio. *IEEE Access*, *10*, 115833-115848. https://doi.org/10.1109/ACCESS.2022.3219090

[5] Al-Makhles, D., Patel, N., & Swain, A. (2013, September). Conventional and hybrid bit-Stream in real-time system. In *2013 Proceedings of the 11th Workshop on Intelligent Solutions in Embedded Systems (WISES)* (pp. 1-6). IEEE.

[6] Arvinth, N. (2024). Challenges of Digital Education in India. *International Academic Journal of Social Sciences*, *11*(1), 01–04. https://doi.org/10.9756/IAJSS/V11I1/IAJSS1101

[7] Asha, S. J., Pai, P., Kamath, P., Madli, R., & Arjunan, R. V. (2024). An Improved EEG Signal Feature Selection Paradigm for Migraine Detection. *Journal of Internet Services and Information Security*, *14*(3), 143-156. https://doi.org/10.58346/JISIS.2024.I3.008

[8] Awad, M., Abougindia, I. T., Elliethy, A., & Aly, H. A. (2021). Flexible architecture for real-time synchronized processing of multimedia signals. *Multimedia Tools and Applications*, *80*(12), 18531-18551.

[9] Batista, A. J. N., Combo, A., Sousa, J., & Varandas, C. A. F. (2002). A distributed, hardware reconfigurable and packet switched real-time control and data acquisition system. *Fusion engineering and design*, *60*(3), 443-448. https://doi.org/10.1016/S0920-3796(02)00045-5

[10] Blackburn, L. C., Golden, E., Wynn, A., Wagner, A., & Gershenfeld, N. (2023). Design and simulation of phase synchronizer for adiabatic quantum flux parametron circuits. *IEEE Transactions on Applied Superconductivity*, *33*(5), 1-5. https://doi.org/10.1109/TASC.2023.3243186

[11] Bondariev, A., Maksymiv, I., & Altunin, S. (2020, February). Simulation and experimental research of the enhanced BPSK and QPSK demodulator. In *2020 IEEE 15th International Conference on Advanced Trends in Radioelectronics, Telecommunications and Computer Engineering (TCSET)* (pp. 767-770). IEEE. https://doi.org/10.1109/TCSET49122.2020.235538

[12] Braojos, R., Bortolotti, D., Bartolini, A., Ansaloni, G., Benini, L., & Atienza, D. (2016). A synchronization-based hybrid-memory multi-core architecture for energy-efficient biomedical signal processing. *IEEE Transactions on Computers*, *66*(4), 575-585. https://doi.org/10.1109/TC.2016.2610426

[13] Chaichomnan, C., & Khumsat, P. (2023). A 1.8 V 25 Mbps CMOS single-phase, phase-locked loop-based BPSK, QPSK demodulator. *International Journal of Electrical and Computer Engineering*, *13*, 6102-6117. https://doi.org/10.11591/ijece.v13i6.pp6102-6117

[14] Chauhan, P., & Bhatia, A. D. (2025). Digital Transformation in Public Sector ICT: A Case Study-Based Comparative Analysis. *International Academic Journal of Innovative Research*, *12*(3), 27-32. https://doi.org/10.71086/IAJIR/V12I3/IAJIR1222

[15] Desai, P., & Joshi, V. (2023). Bridging Traditional and Modern Medical Terminologies Integrative Perspectives from Ayurveda and Allopathy. *Global Journal of Medical Terminology Research and Informatics*, *1*(1), 12-15.

[16] Desai, S., & Iyer, S. (2024). Digital Diplomacy and SDG Advocacy: The Role of Social Media in Global Policy Discourse. *International Journal of SDG's Prospects and Breakthroughs*, 4-6.

[17] Dubey, H., & Thakur, A. (2024). Microfluidic Membrane Devices for Real Time Blood Plasma Separation. *Engineering Perspectives in Filtration and Separation*, 5-8.

[18] Flammini, A., & Ferrari, P. (2010). Clock synchronization of distributed, real-time, industrial data acquisition systems. *Data Acquisition*, 41-62.

[19] Kommangunta, V., Shehzad, K., Verma, D., & Lee, K. Y. (2022, February). Low-Power Light-Weight Binary Phase Shift Keying Demodulator for Magnetic Field Communications. In *2022*

International Conference on Electronics, Information, and Communication (ICEIC) (pp. 1-3). IEEE. https://doi.org/10.1109/ICEIC54506.2022.9748321

[20] Kumar, H. V., Arpana, M. K., Venkatamuni, T., & Rambabu, G. (2022, May). Pulsed BPSK RF Subsystem for X-band Surveillance Radars. In *2022 3rd International Conference for Emerging Technology (INCET)* (pp. 1-4). IEEE. https://doi.org/10.1109/INCET54531.2022.9824301

[21] Lazarovych, I., Kozlenko, M., Kuz, M., Tkachuk, V., Dutchak, M., Savka, I., & Pikuliak, M. (2021, August). Software implemented enhanced efficiency BPSK demodulator based on perceptron model with randomization. In *2021 IEEE 3rd Ukraine Conference on Electrical and Computer Engineering (UKRCON)* (pp. 221-225). IEEE. https://doi.org/10.1109/UKRCON53503.2021.9575458

[22] Lee, S., Hara, S., Dong, R., Takano, K., Amakawa, S., Yoshida, T., & Fujishima, M. (2021, September). A 272-ghz cmos analog bpsk/qpsk demodulator for ieee 802.15. 3d. In ESSCIRC 2021-IEEE 47th European Solid State Circuits Conference (ESSCIRC) (pp. 415-418). IEEE. https://doi.org/10.1109/ESSCIRC53450.2021.9567798

[23] Li, W., Zhang, Q., Zhang, Q., Guo, F., Qiao, S., Liu, S., ... & Heng, X. (2019). Development of a distributed hybrid seismic–electrical data acquisition system based on the Narrowband Internet of Things (NB-IoT) technology. *Geoscientific Instrumentation, Methods and Data Systems*, *8*(2), 177-186. https://doi.org/10.5194/gi-8-177-2019

[24] Li, Y., Shen, X., Zhang, Z., Li, G., Yin, T., Qi, N., ... & Zhang, Z. (2022, November). A 0.004-mm 2 O. 7-V 31.654-μW BPSK Demodulator Incorporating Dual-Path Loop Self-Biased PLL. In *2022 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)* (pp. 569-573). IEEE. https://doi.org/10.1109/APCCAS55924.2022.10090331

[25] Majid, U. M. A, Atan, NA, Rukli, R., & Khan, A.(2024). Framework of Computer Science Learning Through Hybrid Service Learning Oriented Visual Toward the Continuum of Visualization Thinking and Generic Skills. *Indian Journal of Information Sources and Services*, *14*(3), 192-206. https://doi.org/10.51983/ijiss-2024.14.3.25

[26] Malik, H., Rotake, D. R., & Mahajan, M. (2014). Design and Implementation of BPSK Modulator and Demodulator using VHDL. *IOSR Journal of Electronics and Communication Engineering*, *9*(3), 98-105.

[27] Mei, R., Wang, Z., & Hu, W. (2022). Design and implementation of a low-complexity and reconfigurable carrier frequency synchronizer for satellite communications. *IEEE Communications Letters*, *26*(10), 2435-2439. https://doi.org/10.1109/LCOMM.2022.3187530

[28] Ojha, V., & Arora, N. (2024). Sustainable Marketing Strategies in Emerging Economies: Contributions to the Periodic Series in Multidisciplinary Studies. *Digital Marketing Innovations*, 24-29.

[29] Pan, L., Chen, M., Chen, Y., Zhu, S., & Liu, Y. (2021). An energy-autonomous power-and-data telemetry circuit with digital-assisted-PLL-based BPSK demodulator for implantable flexible electronics applications. *IEEE Open Journal of Circuits and Systems*, *2*, 721-731. https://doi.org/10.1109/OJCAS.2021.3119931

[30] Reddy, S., & Mohan, P. (2024). Optimizing Energy Efficiency in Wireless Power Transmission Systems for Industrial Applications. *Association Journal of Interdisciplinary Technics in Engineering Mechanics, 2*(2), 19-23.

[31] Rezvani, A., Mirzaei, A., Mikaeilvand, N., Nouri-Moghaddam, B., & Gudakahriz, S. J. (2025). A Novel Framework For Enhancing Data Collection Macro-Strategies In Heterogeneous Iot Networks Using Advanced Mathematical Modeling. *Archives for Technical Sciences/Arhiv za Tehnicke Nauke*, (33). https://doi.org/10.70102/afts.2025.1833.001

[32] Scofield, A. C., Seller, G. A., Shaw, T. J., Monahan, D. M., & Valley, G. C. (2019, March). Speckle-based BPSK/QPSK demodulator. In *Optical Fiber Communication Conference* (pp. Th2A-38). Optica Publishing Group.

[33] Shah, S., Töreyin, H., Güngör, C. B., & Hasler, J. (2019). A real-time vital-sign monitoring in the physical domain on a mixed-signal reconfigurable platform. *IEEE transactions on biomedical circuits and systems*, *13*(6), 1690-1699. https://doi.org/10.1109/TBCAS.2019.2949778

[34] Shrivastav, P., & Malakar, U. (2024). Exploring Barriers to Medication Adherence Among Patients with Chronic Diseases. *Clinical Journal for Medicine, Health and Pharmacy*, *2*(3), 21-31.

[35] Sondej, T., & Bednarczyk, M. (2024). Ultra-Low-Power Sensor Nodes for Real-Time Synchronous and High-Accuracy Timing Wireless Data Acquisition. *Sensors*, *24*(15), 4871. https://doi.org/10.1109/TIM.2009.2036402

[36] Sourabh, K. S., Deepika, R., Lekshmi, V., Sudhakar, S., & Manikandan, J. (2019, December). Design and Evaluation of BPSK Demodulator using Model based Programming. In *2019 IEEE 16th India Council International Conference (INDICON)* (pp. 1-4). IEEE. https://doi.org/10.1109/INDICON47234.2019.9030277

[37] Sousa, J., Batista, A. J. N., Pereira, R. C., & Varandas, C. (2006). A unified real-time control and data acquisition hardware platform. *Fusion engineering and design*, *81*(15-17), 1853-1858. https://doi.org/10.1016/j.fusengdes.2006.04.038

[38] Sumithra, G., Swaathy, K. M., Vaishali, M., & Basha, S. M. (2019). Real Time Fog Removal with Improved Quality and Accident Prevention Using V2X Communication. *International Journal of Advances in Engineering and Emerging Technology*, *10*(1), 36-45.

[39] Yang, Y., & Fathy, A. E. (2009). Development and implementation of a real-time see-through-wall radar system based on FPGA. *IEEE Transactions on Geoscience and Remote Sensing*, *47*(5), 1270-1280. https://doi.org/10.1109/TGRS.2008.2010251

[40] Zhang, J., Wu, J., Han, Z., Liu, L., Tian, K., & Dong, J. (2013). Low power, accurate time synchronization MAC protocol for real-time wireless data acquisition. *IEEE transactions on nuclear science*, *60*(5), 3683-3688. https://doi.org/10.1109/TNS.2013.2250306

Authors Biography

S. Vinayaka Babu is with over 20 years of experience in product development, business strategy, and application engineering. Working in 4Semi Technology, he has led cutting-edge Embedded and VLSI projects for industrial, defence, and ISRO applications. He previously held key roles at Cypress Semiconductor, Arrow Electronics, and Electro Systems, contributing to global marketing, program management, and innovative hardware design. A recipient of multiple industry recognitions, he holds MTech in VLSI & Embedded Systems, and an MBA from IIM Bangalore. He continues to play a pivotal role in advancing semiconductor innovation.

Dr.S. Safinaz Associate Professor at ECE Dept, SOE Presidency University. A dynamic and versatile personality with 20 years of experience in technical education, Dr. Safinaz S holds a Ph.D. in Image and Video Processing, from Visveswaraya Technological University, Belgaum. She has played various roles in her illustrious career of over two decades that span across establishing various academic and research laboratory units, developing innovative classroom teaching of exceptional quality, and facilitating a high-performance culture. Dr Safinaz S is a talented coalition builder and eminent researcher with diverse research publications – 19 Internation Journals, 6 International Conference, 4 Patents and Research Proposals for VGST in the field of Image and Video Processing, VLSI and embedded Systems, Digital Electronics & Signal Processing, Artificial Intelligence-Machine Learning etc.